

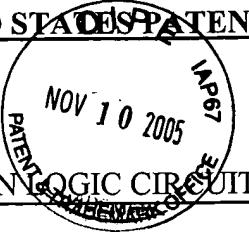
S/N 09/898,752

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sunil Talwar et al.
Serial No.: 09/898,752
Filed: July 03, 2001
Title: MULTIPLICATION LOGIC CIRCUIT

Examiner: David H. Malzahn
Group Art Unit: 2193
Docket: 1365.048US1



INFORMATION DISCLOSURE STATEMENT

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

SUNIL TALWAR ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date

8 Nov. '05

By

Timothy B Clise
Reg. No 40,957

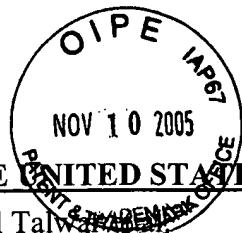
CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 8th day of November, 2005.

PATRICIA A. HULTMAN
Name

Signature

Patricia A. Hultman

S/N 09/898,752



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sunil Talwalkar
Serial No.: 09/898,752
Filed: July 3, 2001
Title: MULTIPLICATION LOGIC CIRCUIT

Examiner: David H. Malzahn
Group Art Unit: 2193
Docket: 1365.048US1

COMMUNICATION CONCERNING RELATED APPLICATIONS

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related applications in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date/Issue Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/637,532 6,938,061	August 11, 2000	1365.033US1	A PARALLEL COUNTER AND A MULTIPLICATION LOGIC CIRCUIT
10/472,658	September 22, 2003	1365.072US1	A MULTIPLICATION LOGIC CIRCUIT
10/714,408	November 14, 2003	1365.063US1	LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicants request that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

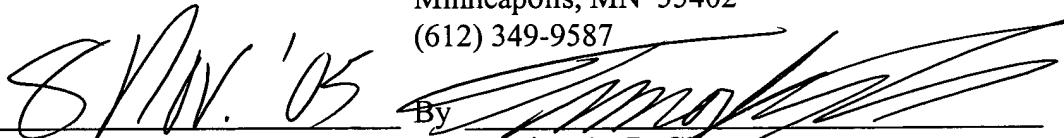
Respectfully submitted,

SUNIL TALWAR ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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By 

Timothy B. Chase
Reg. No. 40,957

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PATRICIA A. HULTMAN

Name


Signature

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <small>(Use as many sheets as necessary)</small>		<i>Complete if Known</i> Application Number 09/898,752 Filing Date July 3, 2001 First Named Inventor Talwar, Sunil Group Art Unit 2193 Examiner Name Malzahn, David	
<small>NOV 10 2005 1AP67 PATENT & TRADEMARK OFFICE</small>		Attorney Docket No: 1365.048US1	
Sheet 1 of 1			

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
	US-2004/0103135A1	05/27/2004	Talwar, S.	09/22/2003
	US-2004/0153490A1	08/05/2004	Talwar, S., et al.	11/14/2003
	US-5,701,504	12/23/1997	Timko, M. A.	12/28/1994
	US-6,938,061	08/30/2005	Rumynin, D., et al.	08/11/2000

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T ²
	GB-2263002	07/07/1993	Poon, J. T.	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		"Communication Pursuant to Article 96(2) EPC, for application No. EP 02 722 402.1, date mailed June 6, 2005", 3 Pages	
		NICHOLSON, J. O., "Parallel-Carry Adders Listing Two-Bit Covers", <u>IBM Technical Disclosure Bulletin</u> , 22(11), (April, 1980), 5036-5037	
		ONG, S. , et al., "A Comparision of ALU Structures for VLSI Technology", <u>Proceedings, 6th Symposium on Computer Arithmetic (IEEE)</u> , (1983), 10-16	
		SCHMOOKLER, M. S., et al., "Group-Carry Generator", <u>IBM Technical Disclosure Bulletin</u> , 6(1), (June, 1963), 77-78	
		SONG, PAUL J., et al., "Circuit and Architecture Trade-offs for High-Speed Multiplication", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 26, No. 9, (September 1991), 1184-1198	
		WEINBERGER, A., "Extension of the Size of Group Carry Signals", <u>IBM Technical Disclosure Bulletin</u> , 22(4), (September, 1979), 1548-1550	
		WEINBERGER, A., "Improved Carry-Look-Ahead", <u>IBM Technical Disclosure Bulletin</u> , 21(6), (November, 1978), 2460-2461	

EXAMINER

DATE CONSIDERED